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Fast hardware-software coverification by optimist execution of real processor

Sungjoo Yoo Jong-Eun Lee Jinyong Jung Kyungseok Rha Youngchul Cho Kiyounc Choi
Sch. of Electr. Eng., Seoul Nat. Univ.;

This paper appears in: **Design, Automation and Test in Europe Conferen and Exhibition 2000. Proceedings**
03/27/2000 -03/30/2000, 2000
Location: Paris, France
On page(s): 663-668
2000
References Cited: 17
IEEE Catalog Number: PR00537
Number of Pages: xxxiv+770
INSPEC Accession Number: 6629194

Abstract:
To achieve fast verification of the software part of an embedded system, we propose to run the target processor optimistically, which effectively reduces t synchronization overhead with other simulators. For the optimistic processor execution, we present a processor execution platform and state saving/restor methods. We performed optimistic execution of ARM710A processor in the coverification of an IS-95 CDMA cellular phone system and obtained up to orc of magnitude higher performance compared with the case that the processor conservatively

Index Terms:
application specific integrated circuits embedded systems formal verification hardware-software codesign integrated circuit design synchronisation ARM710A processor IS-95 CDMA cellular phone system embedded system hardware-software coverification optimistic execution processor execution platform real processor state saving/restoration methods synchronization overhead target processor

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ICEBERG: an embedded in-circuit emulator synthesizer for microcontrollers

Ing-Jer Huang Tai-An Lu
Inst. of Comput. & Inf. Eng., Nat. Sun Yat-Sen Univ., Kaohsiung;

This paper appears in: **Design Automation Conference, 1999. Proceedin 36th**
06/21/1999 -06/25/1999, 1999
Location: New Orleans, LA , USA
On page(s): 580-585
1999
References Cited: 17
IEEE Catalog Number: 99CH36361
Number of Pages: xxxii+1003
INSPEC Accession Number: 6496041

Abstract:
This paper presents a synthesis tool ICEBERG for embedded in-circuit emulat (ICE's), that are part of the development environment for microcontroller (or microprocessor)-based systems (PIPER-II). The tool inserts and integrates th necessary in-circuit emulation circuitry into a given RTL core of a microcontrc and thus turning the core into an embedded ICE. The ICE, based on the IEEE 1149.1 JTAG architecture, provides standard debugging mechanisms, includi boundary scan paths, partial scan paths, single stepping, internal resource monitoring and modification, breakpoint detection, and mode switching betw debugging and free running modes. ICEBERG has been successfully applied t synthesize the embedded ICE for an industrial microcontroller HT48100 from RTL core

Index Terms:
boundary scan testing computer debugging computer testing development systems level synthesis logic testing microcontrollers virtual machines HT48100 ICEBERG 1149.1 JTAG architecture PIPER-II RTL core boundary scan paths breakpoint dete debugging mode development environment embedded in-circuit emulator synthesizer running mode internal resource modification internal resource monitoring microcontrc microprocessor-based systems mode switching partial scan paths single stepping standard debugging mechanisms synthesis tool

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